Memory Combines Parity Checking with Program Tracing Support

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Build-in debugging aids are provided only in high-performance microprocessors (e. g. 80386). Except for that, program tracing requires to rely on expensive external hardware (in-circuit emulators, logic analyzers), especially in real-time embedded systems where software-based methods are not completely adequate.

An inexpensive approach to provide at least address compare stop and instruction step functions can be based on an additional RAM bit position in the memory. During normal operation, this bit position is used for parity checking. Additionally, only a few gates, a program-loadable control register, and activation means for NMI (or for another high-priority interrupt) are required.

The circuitry (see figure) will be described on the basis of the different modes of operation:

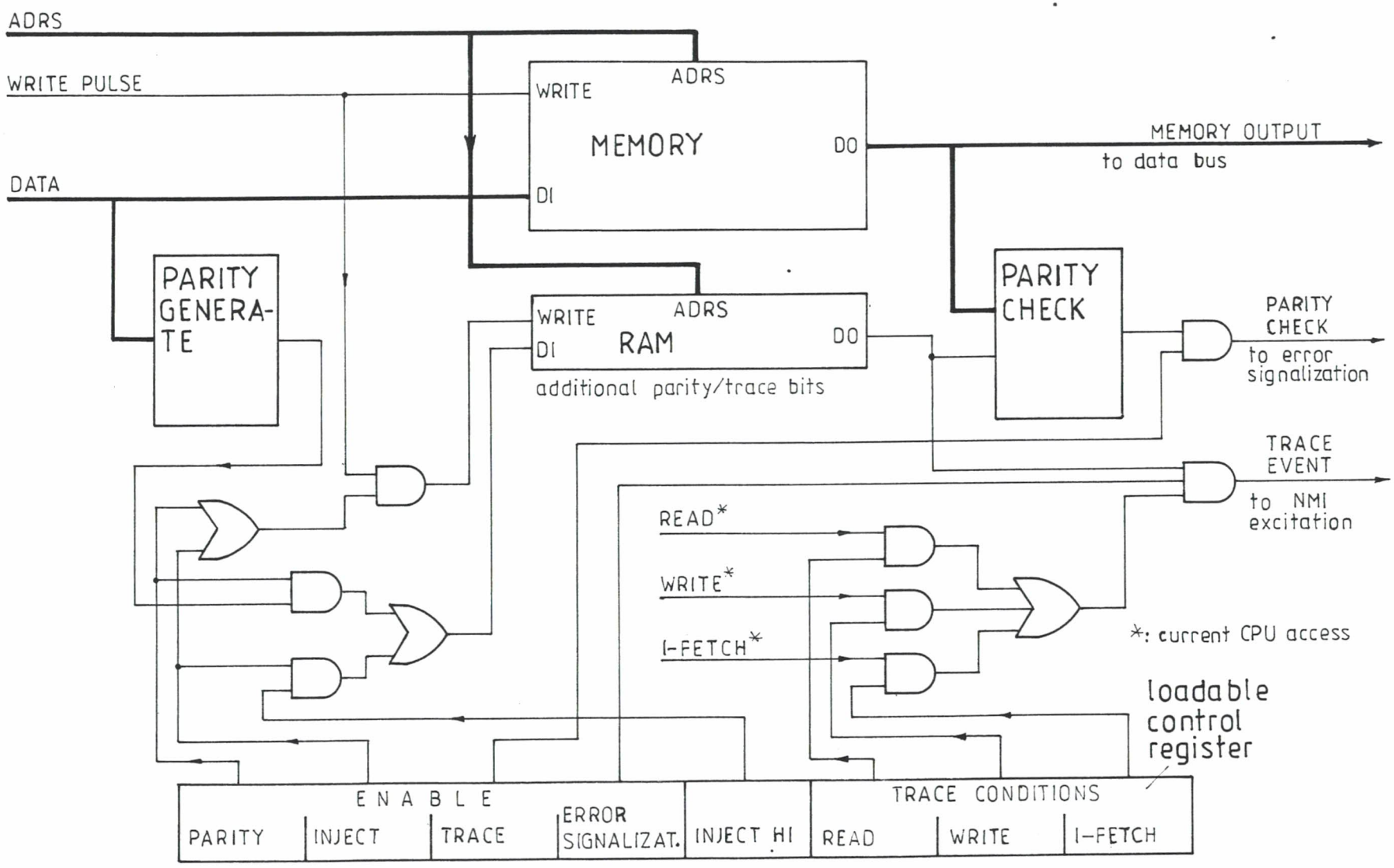
a) Conventional mode. Parity checking is activated. ENABLE PARITY CHECK and ENABLE ERROR SIGNALIZATION are both set. In all write cycles, parity will be written. In all read cycles, parity will be checked.

b) Program tracing mode. Write access to the additional memory bit position is inhibited. A "1" read out of this position will activate NMI, thus triggering the tracing software. ENABLE TRACE must be set. Additional bits may be set to specify the trace condition (e. g. ON I-FETCH, ON READ, ON WRITE).

c) Tracing setup mode. Neither tracing nor parity check are enabled. ENABLE INJECT is set. In write cycles, the value of INJECT HI will be written into the additional RAM. Thus setup software may set or clear, respectively, the desired address positions for tracing. A block move with identical source and destination addresses over the whole address range is sufficient to leave the conventional mode (ENABLE INJECT set, INJECT HI cleared).

d) Conventional setup mode. Parity bits will be written, but parity checking is inhibited. Only ENABLE PARITY is set in the control register. A block move (read and write again) over the whole address range is sufficient to establish the conventional mode.

e) No-effect mode. The control register is cleared completely. The content of the additional memory will be neither affected nor evaluated. This mode is used by diagnostic software. Besides, this state should be reached after hardware reset. Note: After reset, it is necessary to prevent error and trace conditions from being signalized. Thus only ENABLE ERROR SIGNALIZATION and ENABLE TRACE require to be reset by hardware, the remaining bits may be cleared by software.



Memory with parity check/tracing provisions.